



DESIGN OF VITERBI ALGORITHM USING PCAG

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ABSTRACT: The Viterbi algorithm, an application of dynamic programming, is widely used for estimation and detection problems in digital communications and signal processing. It is used to detect signals in communication channels with memory, and to decode sequential error-control codes that are used to enhance the performance of digital communication systems. In architecture of Viterbi algorithm, we are utilizing scheme of polar code address generator which is based on the low complexity and low latency. The main benefit of this proposed system is that it gives reliable requirements and as well as performance degradation. For the motive of bench mark we are improving the both application specific integrated circuit and field programmed gate array. Depend upon the reliability objectives and performance degradation tolerance, the proposed system is utilized.

KEY WORDS: Viterbi algorithm, branch metric unit, state metric unit, trace back unit.

I.INTRODUCTION

The principle plan of this Viterbi calculation is to decipher the convolution codes. Interpreting of this calculation is used in numerous applications, for example, satellite correspondence, cell and radio hand-off. For the most part this Viterbi calculation is actualized with serializer and deserializer imperatives which have basic inertness. This serializer and deserializer are broadly utilized in neighborhood synchronous optical systems. Similarly it is utilized in the attractive stockpiling frameworks like hard circle drive or advanced video plate. This calculation comprises of conceivable number of states [1-3]. Branch metric unit (BMU) and Ad compare select (ACS) and survivor path memory (SPM) are the three segments of Viterbi calculation. Going to the branch metric unit, it creates the measurements which are related to the double trellis and this procedure will rely on the got flag.

Next one is survivor way memory, it deal with the ways and gives the decoded information as yield. An include look at select segment comprises of input circles. By utilizing the cycle plans we can restrict the speed of the framework.

In the Viterbi decoder we are utilizing M- step look forward system to break the emphasis bound. Here the look head strategy will consolidate the few trellises Step to one trellis step. Branch metric pre-

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calculation method will commands the whole multifaceted nature of the framework. For each two back to back strides there are pipelined enlists in the BMP. Include task is performed before the immersion of trills however after the immersion of trills the include activity is trailed by look at activity. In this think about activity we need a parallel way which comprises of less measurements [4].

Convolution encoder can be utilized to improve the addition and to build the scope of inclusion. Generally Viterbi calculation based decoders are utilized to unravel the encoded information. Hence if encoder is used in the transmitter, two Viterbi processors are required, one to perform demodulation and another to decode the detected symbols. This increases the complexity of the receiver design and requires more hardware resources. It would be beneficial if both the detection and decoding can be performed jointly over a single trellis structure. This can be achieved by using a Joint Viterbi Detector and Decoder. The Joint Viterbi Detection and Decoding algorithm comprise of two parts, the metric thresholding part and parity

part. The metric thresholding part calculates the path metrics from the trellis structure for all the possible paths. At each stage of the trellis some paths which are having lower metric values are discarded. This is done to prevent the growth of number of survivors at a faster rate. For this either a threshold value can be set or a maximum number of survivors can be defined. Both these parameters are user defined and latter one is used in this proposed model. At the end of the trellis, multiple survivors are retained and corresponding code words are detected. The parity check part performs the parity check operation $cHT = 0$ where c is code word corresponding to the survivor path and H is the parity check matrix. The code words failing the parity check are discarded and the one that passes the test is selected and decoded [5].

The Viterbi calculation is utilized in convolution codes, this convolution codes creates the yield which corrupt the exactness of translating. Essentially, the mistakes will happen in advanced frameworks in light of rationale delay, alpha particles. In the same way, in advanced process technologies the errors are obtained due to the device shrinking, reduce power supply voltages and higher operating frequencies. Here the energetic protons and electrons are obtained due to the cosmic rays in single transients. So to avoid these errors we use the error detection scheme. This error detection technique is used in hardware architecture with various domains [6-8].

Now, this proposed Viterbi architecture is divided into two approaches for measuring both area and power consumption. By using these approaches we should minimize the efficiency of degradations. After

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this process the signature based approach is followed to get the acceptable efficiency and in the same way to detect the errors that is permanent

and transient errors we should use the encoded operands. Presently to recognize blunders in the ACS we utilize the variations which are recomputed with shift operations (RESO). In a similar method to get the less blames we utilize the recomputed with pivoted operands. In the proposed Viterbi algorithm architecture we use the redundancy techniques.

EXISTED SYSTEM

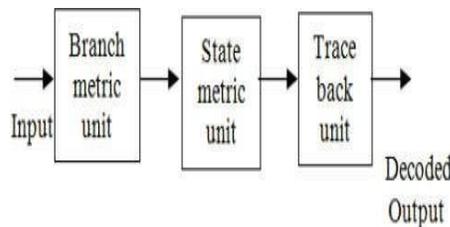


Fig. 1: EXISTED SYSTEM

The above figure (1) shows the architecture of existed system. In this system branch metric unit, state metric unit and trace back unit blocks are used. Coming to branch metric unit it will compute the input value and passes through the state metric unit. Trace back unit of the VD that finds the state with the lowest value and returns the path ending in this state.

A state metric unit condenses branch measurements to get measurements for ways, where K is the limitation length of the code, one of which can in the long run be picked as ideal. Each clock decides, losing wittingly non ideal ways. The consequences of these choices are kept in touch with the memory of a follow back unit. The manner by which they are associated between themselves is characterized by a particular code's trellis chart. Since branch measurements are dependably, there must be an extra circuit (not appeared on the picture) keeping metric counters from flood. An other strategy that takes out the need to screen the way metric development is to

enable the way measurements to "move over"; to utilize this technique it is important to ensure the way metric gatherers contain enough bits to avoid the "best" and "most noticeably terrible" values from drawing near $2(n-1)$ of one another. The think about circuit is basically unaltered. Back-follow unit reestablishes a (nearly) most extreme probability way from the choices made by SMU. Since it does it in backwards heading, a viterbi decoder includes a FILO (first-in- last-out) cushion to remake a right

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request. State metric unit is in charge of monitor the data bits which are connected with the enduring ways. The assignment is finished by the state metric Calculation. In this, a move register is connected with each trellis hub all through the activity of deciphering. Since one of the real advantages is the low power plan. By using the follow back methodology the existed framework scatters the high power. So a new system is proposed which is discussed in below section.

PROPOSED SYSTEM

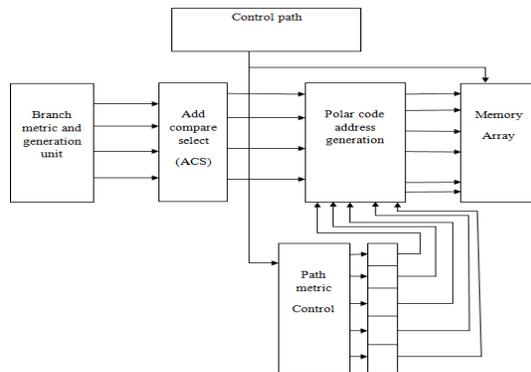


Fig. 2: PROPOSED SYSTEM

The below figure (2) shows the architecture of proposed system. In this system we use branch metric and generation unit, add and compare select, polar code address generation block, path metric control and memory array unit. Here first the branch metric unit will pass the input by generating a sequence. This sequence is followed by add compare select unit. Add compare select unit will compare the obtained values and

now the polar code address generator will generate the address and saves that address in memory cell array. Depend upon the control path the entire operation depends.

The Branch Metric unit (BMU)

A branch metric unit's capacity is to figure branch measurements, which are normed separates between each conceivable image in the code letters in order, and the got image. This is commonly founded on a look-into table containing the different piece measurements. The PC looks into the n-bit measurements related with each branch and aggregates them to get the branch metric. The outcome is passed along to the way metric Calculation. The obligation of this unit is to figure the Hamming code between the normal code and the accepting code as a casing. At each preparing, the BMU finds the Hamming code for these images.

Path metric unit

The path metric circuit comprising of adders, a comparator, a selector, and a few registers ascertains the way metric of every convolution code state. The quantity of "states" N, of a convolution encoder



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